16.3 On-Die Supply-Voltage Noise Sensor with Real-Time Sampling Mode for Low-Power Processor Applications

Tomio Sato[1], Atsuki Inoue[1], Tetsuyoshi Shiota[1], Tomoko Inoue[1], Yukihito Kawabe[1], Tetsutaro Hashimoto[1], Toshifumi Imamura[2], Yoshitaka Murasaka[2], Makoto Nagata[2], Atsushi Iwata[2]

[1]Fujitsu Laboratories, Kawasaki, Japan
[2]A-R-Tec, Higashihiroshima, Japan

To meet the increasing demand for lowering the power consumption of microprocessors, voltage and frequency scaling schemes have been proposed for low-power processors. With these techniques, as power consumption can be lowered at a lower supply voltage, the operating voltage margin should be minimized. However, this increases the risk of malfunction or performance degradation due to large supply voltage noise caused especially by operational mode switching accompanied with frequency changes, such as switching to low power mode [1]. This is because a large transient change in current occurs at this mode switching. However, this type of noise does not occur so frequently, rather once in a long while and this feature makes noise detection very difficult. It is also difficult for designers to predict supply-voltage noise at the design stage as it requires the simulation of long test vectors. Due to the increased integration density and complex operation of processors, detecting such low frequency failures and acquiring statistical information of supply voltage noise are becoming more important than ever.

Several on-die noise sensors have been proposed to measure supply voltage fluctuations [2-4]. Figure 16.3.1 shows that the operating principle of these sensors is based on equivalent sampling, which makes it difficult to detect the supply noise peak within a reasonable time as it rarely occurs during the sampling operation. The equivalent sampling method assumes that the noise waveform is periodic and requires several hundreds of samples to obtain the noise waveform. Another noise sensor based on a ring oscillator has also been proposed [5], but the bandwidth of a voltage sensor based on the ring oscillator is not sufficiently large to detect a sharp noise peak within 5ns. There is thus a strong need for a peak noise detection method with continuously running processors that still has sufficient bandwidth to detect sharp noise peaks [6].

To meet these requirements, we propose a noise-sensing scheme with a real-time sampling mode, as shown in Fig. 16.3.2. Our strategy for detecting the peak supply noise is as follows. First, we take a histogram of each supply voltage to determine the appropriate detection window in advance. The noise peak must be within the tail of this histogram, as marked by A, B, and C in the figure. This is because detecting the processor cycles whose noise peak exceeds a certain value greatly reduces the amount of noise information. Then we measure the peak noise waveform in real time while running the processors. This strategy has two advantages. First, the number of voltage comparators in the ADC is greatly reduced as we can set the detection window to be sufficiently narrow in advance. Second, we use a narrower I/O bandwidth as the amount of noise information is also greatly reduced.

Figure 16.3.3 shows the block diagram of the proposed on-die noise sensor. There are three main blocks: the sensor head block, the peak detection and store block, and the histogram counter block. The peak detection and store block is composed of a memory and a peak search circuit. The peak search circuit finds whether detected data are within the detection window or outside of it, and generates write-enable pulses to memory. The memory records cycle information from the 64b timer and program counter of the processor as well as supply noise level so that the waveform can be played back. The cycle information when noise peaks are detected is used for debugging or processor code morphing for reducing noise peaks. The histogram counter block is composed of a decoder and several counters. The decoder identifies the voltage level of the output from the sensor head and the corresponding counter is incremented at every cycle. To support the conventional equivalent sampling mode, we add two counters and a programmable delay circuit to the controller. Figure 16.3.4 shows the relationship between the frequency of noise events and required I/O bandwidth. Noise events of operational mode switching are more important as larger noise occurs [1]. The switching frequency in low power mode or standby mode is low enough to implement the supply noise capture circuits with a 400kb/s serial interface, such as I2C, assuming the burst length of noise events is 50.

Six conventional comparators [3] and six 8b DACs are implemented in the sensor head as shown in Fig. 16.3.5. The sensor head operates like a flash ADC but with the number of comparators reduced from 256 to 6, owing to searching the detection window before measurement. Conventional level shifters [3] are placed in front of the ADCs to measure various supply voltage levels such as V_{DE}, V_{DD} and V_{SS}. Using SW1 through SW3, we configure this sensor head into on of two modes. In the first mode, upon turning SW2 on, all comparators are connected to the same sensing node so that the signal level is compared with six different voltage levels simultaneously. In the second mode, upon turning SW2 off, 6 comparators are divided into two groups; the upper three comparators measure V_{DE} or V_{DD}, and the lower three comparators measure V_{SS} so that V_{SS} and V_{DD} nodes can be measured simultaneously. Simulation verifies the bandwidth of 700MHz, full range of ±1V, minimum resolution of 10mV, and power consumption of 30mW. The absolute reference level for measurement is chosen to be external GND or PCB GND, because the noise levels of all power lines including V_{SS} are required.

Figure 16.3.7 shows a die micrograph of the test chip implemented in 90nm CMOS. The chip includes two sensor heads, the sensor head controller, the core noise source and the I/O noise source. The sensor head including current source for DACs measures 356×332mm^2. The controller includes 31K gates, and a 1k×96 SRAM. The core noise source consists of several inverter chains and its activation ratio is controllable. The maximum power of the core noise source is 1.0W at a clock speed of 480MHz. The I/O noise source includes 14 I/O buffers.

Figure 16.3.6 shows the measured noise histogram and waveform when core noise is applied. The activation ratio of the core noise source changes from 0% to 75% at every 10ms. In histogram mode, the data set into DACs are scanned from -0.1 to 0.1V for V_{SS} measurement and from 0.8 to 1.3V for V_{DD} measurement. The difference between two peaks for both the V_{DD} and V_{SS} histograms shows IR drop caused by different active current: IR drops of 220mV for V_{DD} and 40mV for V_{SS}. This change of activation ratio also generates large noise peaks owing to a package-die resonance mode as shown in this figure. In the captured histogram, the noise peaks appear at 860mV for V_{DD} and at 50mV for V_{SS}. We have set the noise detection window to 860 to 910mV for V_{DD}, and 40 to 90mV for V_{SS}. The waveform around noise peak are successfully captured at a 480MHz sampling rate for both power lines using real time sampling mode even though the noise event occurs at a 10ms interval.

Acknowledgements:
The authors thank R. Sasagawa, H. Okano and H. Matsuura for test chip implementation and evaluation.

References:
[1] E. Hailu D. Boerstler, D. Miki, et al., "A Circuit for Reducing Large Transient Current Effects on a Processor Power Grid," *ISSCC Dig. of Tech. Papers,* pp. 548-549, Feb., 2006
[2] M. Nagata, K. Hijikata, J. Nagai, et al., "Reduced Substrate Noise Digital Design for Improving Embedded Analog Performance," *ISSCC Dig. of Tech. Papers*, pp. 224-225, Feb., 2000
[3] M. Nagata, T. Okumoto, K. Taki, "A Built-in Technique for Probing Power Supply and Ground Noise Distribution Within Large-Scale Digital Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 813-819, Apr., 2005
[4] M. Takamiya and M. Mizuno, "A Sampling Oscilloscope Macro Toward Feedback Physical Design Methodology," *Symp. VLSI Circuits,* pp. 240-243, Jun., 2004
[5] Y. Kanno, Y. Kondoh, T. Irita, et al., "In-Situ Measurement of Supply-Moise Maps with Millivolt Accuracy and Nanosecond-Order Time Resolution," *Symp. VLSI Circuits Digest of Tech. Papers,* pp. 78-79, Jun., 2006
[6] A. Muhtaroglu et al., "On-Die Droop Detector for Analog Sensing of Power Supply Noise," *IEEE Journal Solid-State Circuits*, vol. 39, no. 4, pp. 651-660, Apr., 2004.

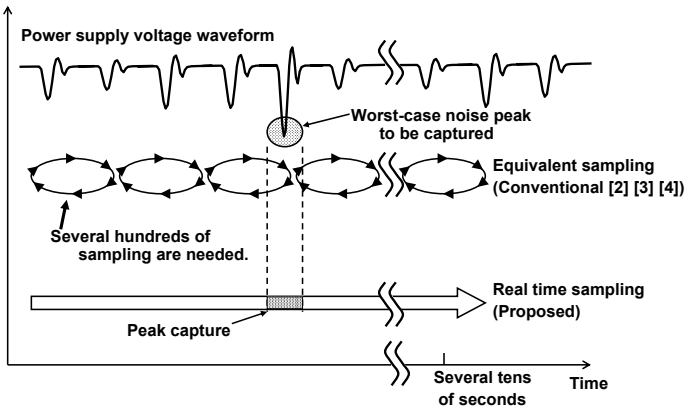


Figure 16.3.1: How to capture the worst-case noise peak.

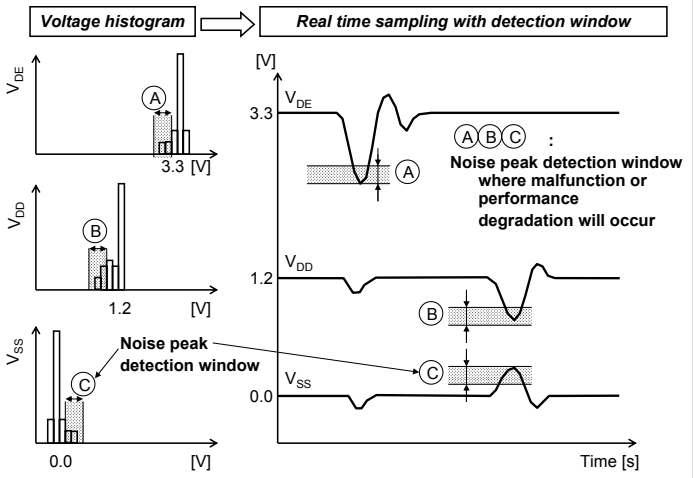


Figure 16.3.2: Strategy of real-time sampling with noise peak detection window.

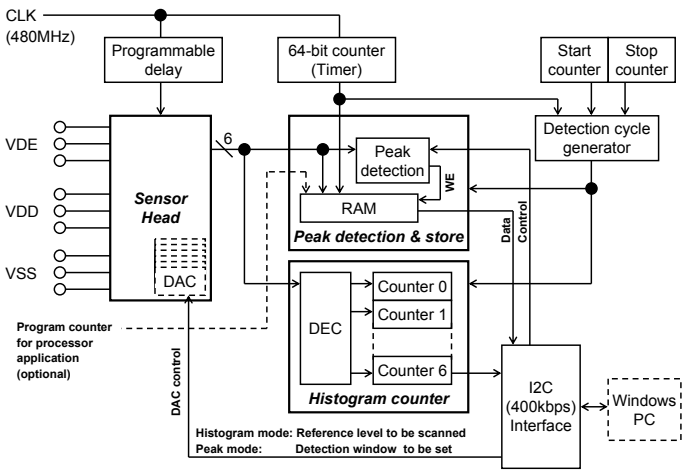


Figure 16.3.3: Block diagram of on-die noise sensor.

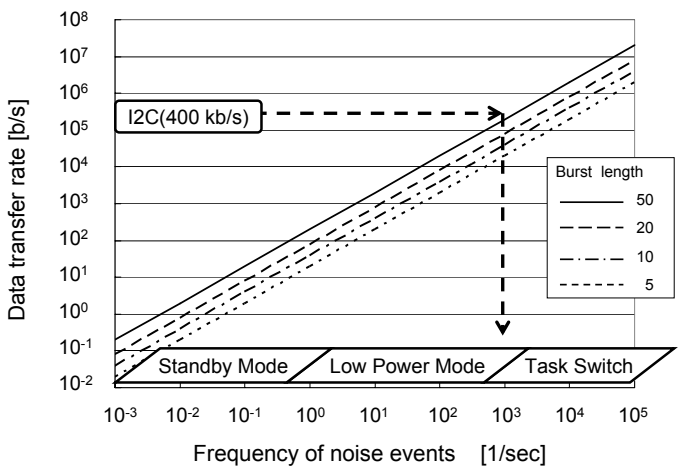


Figure 16.3.4: Required data transfer rate.

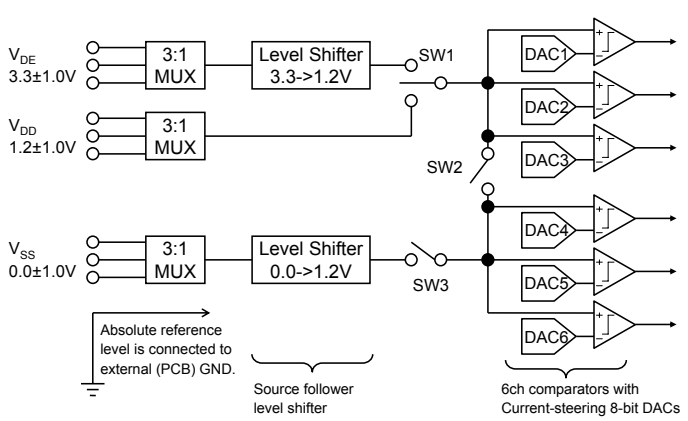


Figure 16.3.5: Noise sensor head implementation.

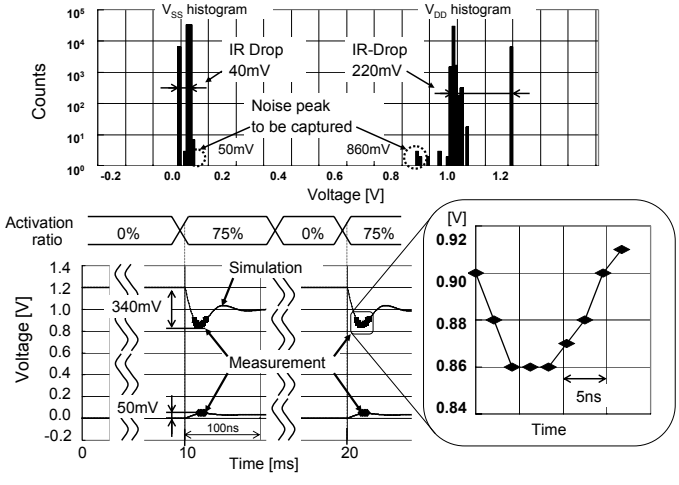
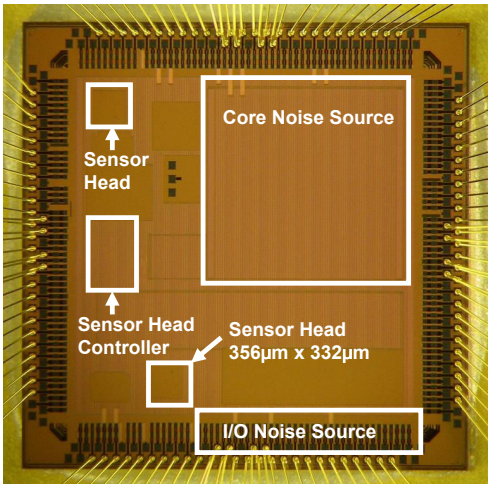


Figure 16.3.6: Experimental result of peak detection.

Continued on Page 603



Process:
90nm CMOS

Die Size:
5.0×5.0mm^2

Sensor Head Size:
356×332µm^2

Power of Sensor Head:
30mW @ 480MHz

Bandwidth:
700MHz

Resolution:
10mV

Full Range:
+/-1V

Figure 16.3.7: Die micrograph of test chip.

